AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 26 without prejudice. Please add new claims 28-29.

1. (CURRENTLY AMENDED) A time-shifted video method comprising the steps of:

a first buffering of an input signal having a digital
video format;

compressing said input signal substantially simultaneously with said buffering, said compressing including a second buffering of said input signal;

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in a real-time mode, delivering a plurality of real-time video frames along a first processing path to an output for display in response to said input signal as first buffered;

in a time-shifted mode, delivering a plurality of time-shifted video frames along a second processing path to said output for display in response to said input signal as compressed, said time-shifted video frames being delayed relative to said real-time video frames; and

pausing at a particular one of said real-time frames during a transition from said real-time mode to said time-shifted mode.

2. (PREVIOUSLY PRESENTED) The method of claim 1, wherein said transition is between said particular real-time frame and a time-shifted version of said particular real-time frame.

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3. (PREVIOUSLY PRESENTED) The method of claim 1, further comprising providing trick functions during the timeshifted mode.

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- 4. (CURRENTLY AMENDED) The method of claim 1, wherein said transition is triggered by a $\underline{\text{single}}$ command of a viewer.
- 5. (PREVIOUSLY PRESENTED) The method of claim 1, wherein the real-time video frames are derived from uncompressed video.

6. (CANCELED)

7. (PREVIOUSLY PRESENTED) The method of claim 1,
20 wherein said real-time video frames are derived from said input
signal having a compressed video format.

- 8. (PREVIOUSLY PRESENTED) The method of claim 7, wherein said real-time video frames are provided from a decoder that decompresses said input signal.
- 9. (PREVIOUSLY PRESENTED) The method of claim 1, wherein the real-time mode, the time-shifted mode, and the transition are provided by a single codec chip.
- 10. (PREVIOUSLY PRESENTED) The method of claim 8,10 wherein said input signal comprises MPEG video.
 - 11. (CURRENTLY AMENDED) The method of claim 1, wherein (i) information is stored identifying said particular real-time video frame and (ii) before the time-shifted mode occurs, a next frame of said time-shifted video frames in display sequence after said particular real-time video frame is queued up for display such that said transition is from said particular real-time video frame to said next frame of said time-shifted video frames.
 - 12. (CANCELED)

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13. (CANCELED)

- 14. (PREVIOUSLY PRESENTED) The apparatus according to claim 22, wherein said real-time decoder and said time-shifted decoder are provided in a single codec.
- 15. (PREVIOUSLY PRESENTED) The apparatus of claim 23, having a first processing path for said real-time mode and a second processing path for said time-shifted mode.

16. (CURRENTLY AMENDED) The apparatus of claim 21, wherein an the encoder and the time-shifted decoder are provided in a single codec.

17. (CANCELED)

- 18. (PREVIOUSLY PRESENTED) The apparatus of claim 23, wherein the apparatus comprises a set-top box.
- 19. (PREVIOUSLY PRESENTED) The apparatus of claim 23, wherein said output signal is viewable by an analog television.
 - 20. (CURRENTLY AMENDED) An apparatus comprising:

a real-time decoder configured to (i) generate a first output signal in response to by decompressing a compressed digital

video input signal and (ii) pause a frame of said first output signal during a transition from a first mode to a second mode;

a frame storage system configured to store said compressed digital video <u>input</u> signal separately from said realtime decoder;

a time-shifted decoder (i) coupled to said frame storage

10 system and (ii) configured to generate a second output signal in

response to said compressed digital video input signal stored in

said frame storage system; and

a controller configured to generate a command configured to control presenting (i) said first output signal when in said first mode and (ii) said second output signal when in said second mode.

21. (CURRENTLY AMENDED) An apparatus comprising: an input for receiving a video signal in an uncompressed

format;

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a frame buffer directly connected to said input and configured to (i) generate a first output signal by buffering said video signal and (ii) pause said first output signal at a frame during a transition from a first mode to a second mode;

an encoder configured to generate a first intermediate signal by compressing said video signal;

a controller separate from said encoder and configured to

(i) receive said first intermediate signal and (ii) present a

second intermediate signal;

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a frame storage system directly connected to said input controller and configured to (i) store said video first intermediate signal separately from said frame buffer and (ii) generate said second intermediate signal; and

a time-shifted decoder <u>separate from said controller and</u> configured to generate a second output signal in response to said video signal stored in said frame storage system; and a <u>by</u> decompressing said second intermediate signal, wherein said controller <u>is further</u> configured to generate a command configured to control presenting (i) said first output signal when in said first mode and (ii) said second output signal when in said second mode.

22. (PREVIOUSLY PRESENTED) An apparatus comprising:

a controller configured to receive (i) a first command and (ii) a video input signal in a compressed format;

a real-time decoder configured to (i) generate a first output signal in response to decompressing said video input signal and (ii) pause a frame of said first output signal during a transition from a first mode to a second mode;

a frame storage system coupled to said controller to exchange said video input signal; and

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a time-shifted decoder coupled to said controller and configured to generate a second output signal in response to (i) said video input signal received from said controller and (ii) said first command;

wherein said controller is further configured to generate a second command to control presenting (i) said first output signal when in said first mode and (ii) said second output signal when in said second mode.

23. (CURRENTLY AMENDED) An apparatus comprising:

a <u>first</u> frame buffer configured to (i) generate a first signal in response to <u>and a second signal by buffering</u> an input signal having a digital format and, (ii) pause said first signal at a frame during a transition from a real-time mode to a time-shifted mode <u>and (iii) buffer a third signal;</u>

a controller connected to said first frame buffer to receive said third signal;

a buffer connected to said controller to store said third signal;

an encoder <u>connected to said first frame buffer and</u> configured to generate a second <u>said third</u> signal <u>by compressing</u> <u>said second signal</u> <u>in response to said input signal</u>, <u>wherein said</u>

second signal is (i) stored in said buffer and (ii) retrieved after
being stored;

a decoder configured to generate a fourth signal by decompressing said third signal as retrieved from said buffer; and

a switch <u>connected to said first frame buffer and</u> configured to present an output signal comprising (i) said first signal when in said real-time mode and (ii) said <u>second fourth</u> signal <u>retrieved from said buffer</u> when in said time-shifted mode.

- 24. (ORIGINAL) The method according to claim 2, wherein said transition is seamless to a viewer.
- 25. (PREVIOUSLY PRESENTED) The method of claim 1, wherein said transition is triggered by an event generated by software.

26. (CANCELED)

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27. (PREVIOUSLY PRESENTED) The apparatus according to claim 22, further comprising a demultiplexer configured to demultiplex said video input signal to said real-time decoder and said controller.

28. (NEW) The apparatus according to claim 21, wherein said encoder receives said video signal from said frame buffer.

29. (NEW) The apparatus according to claim 23, further comprising a second frame buffer disposed between said controller, said time-shifted decoder and said switch and configured to (i) buffer said third signal retrieved from said buffer and (ii) buffer said fourth signal prior to said switch.